

# Design Study for Stacked MEMS

J.E Bullema, M.H.H. Meuwissen, E.P. Veninga

TNO Industrial Technology  
P.O. Box 6235, NL 5600 HE Eindhoven, The Netherlands  
Telephone +31 40 2650488 Fax +31 40 2650305 E-mail [j.bullema@ind.tno.nl](mailto:j.bullema@ind.tno.nl)

## Abstract

This paper describes a design study for a stacked MEMS packaging concept that is able to meet CSP requirements. Within this concept a diversity of materials and technologies can be applied. Numerical simulations are performed to study the performance of the basic elements in this concept. These simulations focus on the thermal and impact behaviour.

## 1. Introduction

Cost effective packaging is considered as a major bottleneck for many new MEMS applications. An important issue in MEMS packaging is the absence of a generalised standard solution for the packaging of basic MEMS functionality.

Based upon analysis of functional requirements of existing MEMS products the authors have developed a packaging concept for MEMS that offers a standard solution for packaging of MEMS functionality.

## 2. The 3D MSP concept

In the current study a stackable packaging concept for MEMS is presented. This concept is called 3D MEMS Scale Package (3D MSP) and is able meet CSP requirements. Figure 1 schematically shows a stack of four chips.

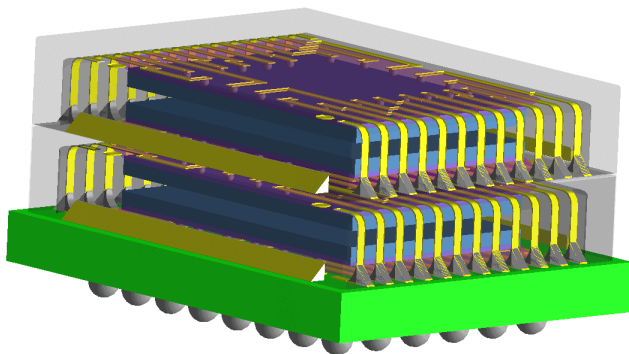


Figure 1: The 3D MEMS Scale Packaging Concept: a stack of four chips.

In the 3D MSP concept, the footprint of the stackable system is slightly larger than that of the dies used. This enables a high degree of miniaturisation.

Microsystems can be build up from several stacked layers, which makes it possible to incorporate additional functional elements (like sensors and actuators) in the system.

Within the concept, a diversity of materials and technologies can be applied. Here, the thermal and mechanical behaviour of the basic components is studied by means of numerical simulations as a first step towards optimal thermal and mechanical performance.

## 3. Numerical simulation of the thermal behaviour of MSPs

In order to assess the thermal performance of some variants of the MSP concept, numerical simulations are performed. The simulations focus on determining the temperature distribution in a package during operation. The influence of several components such as copper tracks and vias on the thermal performance is assessed.

### Governing equations

It is assumed that the thermal behaviour of the individual components in an assembly can be described using Fourier's law [1,2]:

$$q = -\lambda \nabla T. \quad (1)$$

In this equation,  $q$  is the heat flow,  $\lambda$  the heat conductivity, and  $\nabla T$  the temperature gradient. The temperature field is determined by solving the diffusion-equation for a given set of initial conditions and boundary conditions:

$$\rho c_p \frac{\partial T}{\partial t} = -\nabla \cdot q, \quad (2)$$

where  $\rho$  is the density,  $c_p$  the heat capacity, and  $t$  the time. For the current simulations, all parameters are taken constant.

The maximum temperatures occurring in an assembly are to a large extent determined by the ability of the assembly to drain away heat to the environment. Generally, three different interaction principles can be discerned: conduction, convection and radiation. For the current application, it is assumed that the assembly cannot exchange heat with its environment by conduction.

Heat flow due to radiation  $q_R$  is taken into account by the following equation [2]:

$$q_R = \sigma \cdot \varepsilon \cdot (T_S^4 - T_A^4), \quad (3)$$

where  $T_S$  is the surface temperature,  $T_A$  ambient temperature,  $\sigma$  Stefan-Boltzmann's constant and  $\varepsilon$  the emissivity. The value of the emissivity depends on the material composition of the surface.

Heat flow due to convection  $q_C$  is taken into account using the following equation [2]:

$$q_C = h(T_S - T_A), \quad (4)$$

where  $h$  is the film coefficient. The film coefficient is determined by the characteristics of the convection flow

at hand. For typical dimensions of the investigated package and assuming natural convection, the film coefficient is estimated at  $20\text{W/m}^2\text{K}$  [2].

### Investigated assembly

A typical chip-carrier placed on a substrate consists of a multitude of design features made of different materials each with its own (thermal) characteristics. The properties of the individual features and their mutual interactions result in a particular thermal behaviour of the whole assembly.

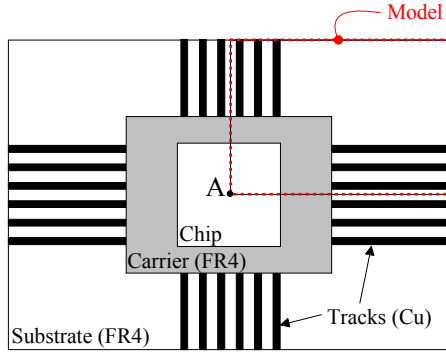


Figure 2: Schematic drawing (top view) of the assembly for which influence of different components on the thermal performance is investigated. The modelled part is indicated by the dashed line.

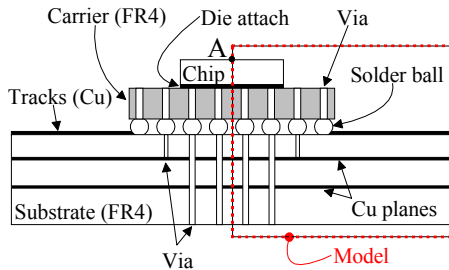


Figure 3: Schematic drawing (cross section) of the assembly.

The contribution of the individual features on the thermal performance is investigated using the assembly schematically drawn in Figure 2 and Figure 3. It consists of a chip ( $5 \times 5 \times 0.3\text{mm}^3$ ) placed on an FR4 carrier ( $8 \times 6 \times 0.5\text{mm}^3$ ) which is placed on an FR4 substrate (1.6mm thickness). The thickness of the die attach layer between the chip and the carrier is  $30\mu\text{m}$ .

The electrical interconnects between the carrier and the substrate are established via a  $6 \times 8$  matrix of  $500\mu\text{m}$  solder balls that are placed at a  $750\mu\text{m}$  pitch. Furthermore, different types of vias are present in the carrier and the substrate.

Because of the poor thermal conductivity of the FR4 material, the influence of different features in the FR4 substrate on the thermal performance is investigated by means of simulations.

### Model and boundary conditions

A model of the assembly is implemented in the finite element package MSC.Marc [3]. Because of symmetry reasons, only a quarter of the assembly is modelled (see Figure 2 and Figure 3). Figure 4 shows the finite element mesh. The mesh consists of approximately 5700 linear isoparametric brick elements and 7200 nodes.

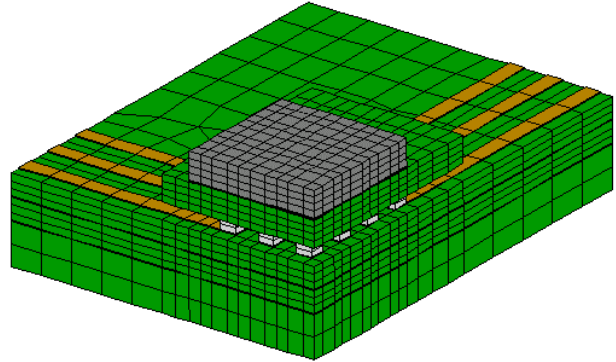


Figure 4: Finite element model of a quarter of the assembly.

The symmetry planes and outer boundaries of the substrate are assumed to be isolated from the environment. At the other surfaces in contact with air, combined convection and radiation heat exchange is assumed. The assembly is initially at room temperature (293K) and at  $t=0.0\text{s}$  the chip starts dissipating heat at a rate of  $1.0\text{W}$ .

### Material properties

All materials in the assembly are assumed to behave according to Fourier's law. The parameters for the individual materials are summarised in Table 1.

Table 1: Materials' properties used for the finite element analyses of the thermal behaviour.

Material	Conductivity [W/mK]	Density [kg/m <sup>3</sup> ]	Heat Capacity [J/kg/K]
Silicon	$1.5 \cdot 10^{-2}$	$2.3 \cdot 10^{-3}$	$7.6 \cdot 10^{+2}$
FR4	$2.0 \cdot 10^{-1}$	$2.6 \cdot 10^{+3}$	$8.4 \cdot 10^{+2}$
Die attach	$1.5 \cdot 10^{+0}$	$1.1 \cdot 10^{-4}$	$2.4 \cdot 10^{+2}$
Copper	$3.9 \cdot 10^{+2}$	$8.9 \cdot 10^{+3}$	$3.9 \cdot 10^{+2}$
Solder	$5.1 \cdot 10^{+1}$	$8.4 \cdot 10^{+3}$	$1.9 \cdot 10^{+2}$

### Results

The following configurations are analysed:

1. No design features (Cu planes, vias, tracks) in or on the FR4 substrate.
2. As 1 with inclusion of Cu planes in the substrates at the locations indicated in Figure 3.
3. As 2 with addition of Cu tracks on the substrate's top surface (see Figure 2).
4. As 3 with inclusion of vias to the two Cu planes and the back surface of the substrate (see Figure 3).

Figure 5 shows the temperature distribution in the assembly after 300 seconds for configuration 1 (no features in substrate). For this situation, the chip attains a maximum temperature of around 550K (277°C) which is unacceptably high. Furthermore, strong temperature gradients are visible in the substrate caused by the poor conductivity of this material. On the other hand, the temperature gradients over the thickness of the FR4 carrier are relatively small due to the presence of vias that act as thermal pathways.

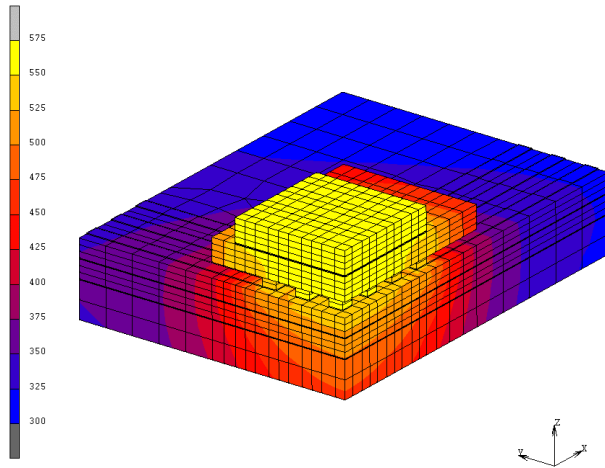


Figure 5: Temperature distribution (in K) in the assembly after 300 seconds without any components in the substrate (configuration 1).

Figure 6 shows the temperature as a function of time for the four configurations. A steady state temperature distribution is attained after approximately 300 seconds.

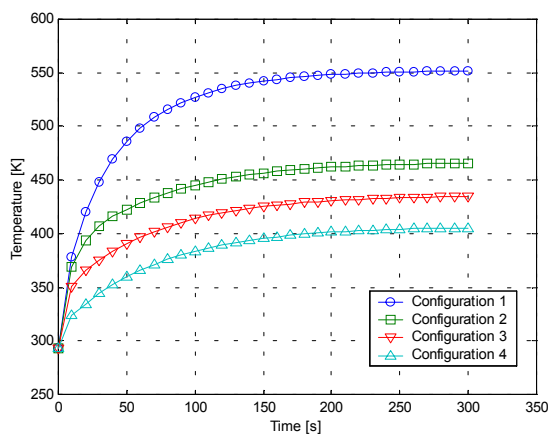


Figure 6: Temperature history at the centre of the chip (point A, see Figure 2) for configuration 1 to 4.

The addition of the Cu planes (thickness 18µm) leads to a significant improvement of the thermal performance. The maximum temperature in the centre of the chip is reduced by about 100K. Inclusion of vias and tracks in and on the substrate result in a further reduction of the peak temperature by 60K. Nevertheless, the maximum temperature of approximately 400K (130°C) is still unacceptable. Therefore, it must be concluded that the

power dissipation of the chip (1W) is too high for this configuration.

### Thermal performance of a stacked package

The simulations of the previous section were carried out on an assembly containing one chip. The packaging concept however allows for a stackable configuration. In order to investigate the influence of several chips packed close together, some simulations are performed.

Figure 7 shows a cross-section of the stacked chip configuration consisting of two chips placed in an alumina housing which is attached to an alumina carrier. This assembly is placed on an FR4 substrate. The housing has dimensions of 7.6×5.6×2.0mm<sup>2</sup>. The solder balls used for chip to housing interconnects and chip to carrier interconnects are 130µm in diameter and are placed at a 500µm pitch.

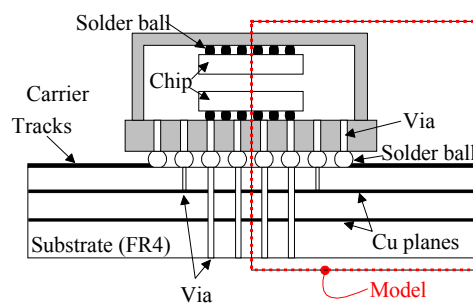


Figure 7: Cross-section of the stacked chip configuration.

### Model and boundary conditions

The finite element mesh of the assembly is shown in Figure 8. As for the previous simulations, only a quarter of the assembly is modelled because of symmetry. The mesh consists of 7000 linear isoparametric brick elements and 9000 nodes.

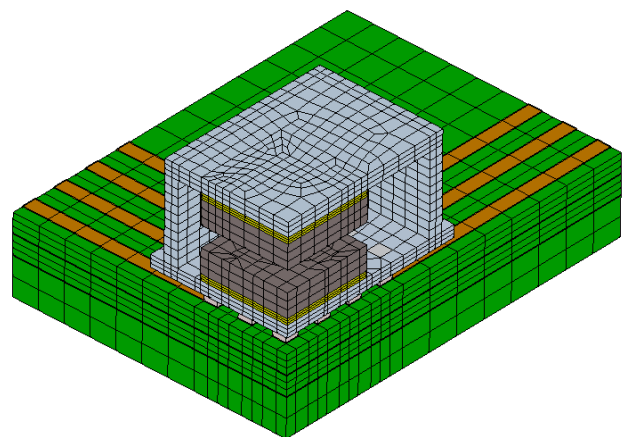


Figure 8: Finite element mesh of the assembly containing 2 stacked chips.

All symmetry planes are assumed to be isolated from the environment. Heat exchange at the surfaces in contact with air is established via radiation and convection. The whole assembly is initially at room temperature and at  $t=0.0s$  the two chips start dissipating heat.

All materials are assumed to behave according to Fourier's law. The materials' parameters are summarised in Table 1 and Table 2.

Table 2: Materials' properties used for the housing materials in the finite element analyses of the thermal behaviour of the stacked assembly.

Material	Conductivity [W/mK]	Density [kg/m <sup>3</sup> ]	Heat Capacity [J/kg/K]
PA6	$2.5 \cdot 10^{-1}$	$1.1 \cdot 10^{+3}$	$1.6 \cdot 10^{+3}$
Al <sub>2</sub> O <sub>3</sub>	$2.5 \cdot 10^{+1}$	$3.8 \cdot 10^{+2}$	$8.0 \cdot 10^{+2}$

## Results

Figure 9 shows the temperature distribution at  $t=500s$  for the situation in which each chip dissipates heat at a 1.0W rate. For this package, this dissipation power is clearly too high. Especially the upper chip is heated up excessively (to approximately 535 K).

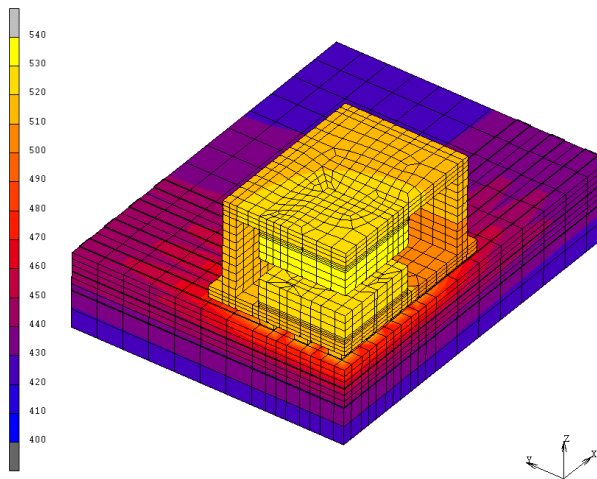


Figure 9: Temperature distribution in the assembly at  $t=500s$  for two chips producing 1W heat each.

Reduction of the heating power to 0.1W for both chips results in a reduction of the maximum temperature in the upper chip by more than 200K (to 320K).

The housing material chosen for the current simulations was the relatively well conducting alumina. Changing the housing material from alumina to a PA6 polymer leads to much stronger temperature gradients due to the poor thermal conductivity of this material (see Figure 10). The maximum temperature of the upper chip is approximately 390 K while that of the lower chip attains approximately 310 K.

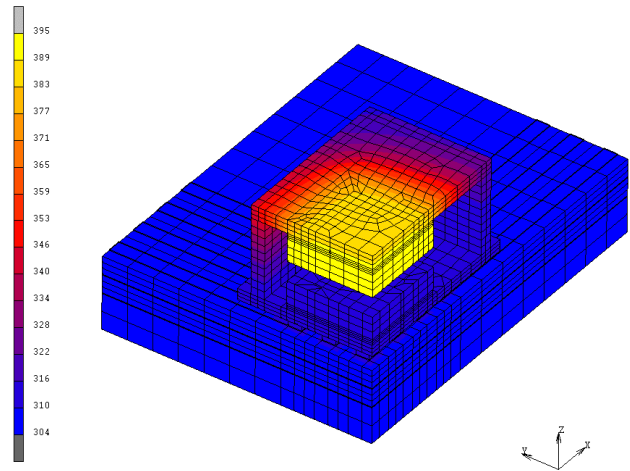


Figure 10: Temperature distribution in the assembly at  $t=500s$  for two chips producing 0.1W heat and a PA6 polymer housing.

## 4. Numerical simulation of the mechanical behaviour of MSPs

Next to the thermal behaviour, the mechanical behaviour of the 3D MSP concept deserves special attention. This includes both thermo-mechanical reliability (especially of the interconnects) and impact resistance, which might be more critical for this kind of package due to the greater stacking height compared with standard packages.

### Model and boundary conditions

For the initial impact analysis a simple plane strain model is implemented (see Figure 11). The model shown in this figure consists of a housing with two chips attached to a substrate by solder interconnects.

The model consists of approximately 1000 bilinear isoparametric quad elements. A Houbolt time integration scheme is adopted to solve the system of equations using a  $1.0 \cdot 10^{-6}$  seconds time step.

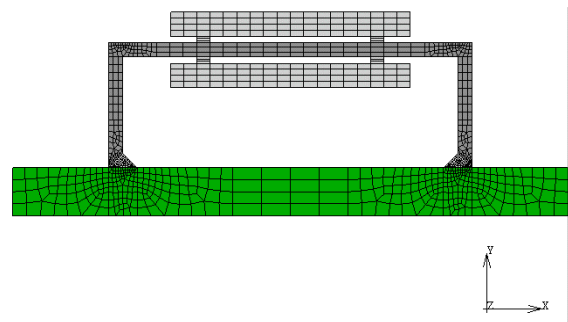


Figure 11: Plane strain model of a housing on a carrier and two chips for impact simulations. The vertical line on the right denotes the floor.

The assembly has an initial velocity of 5.4m/s in positive  $x$ -direction, corresponding to a drop height of 1.5m. The gravity force is acting in positive  $x$ -direction. The solder material behaviour is described using a time independent elasto-plastic model with Von Mises yield criterion,

associated plastic flow and piecewise linear hardening [4]. All other materials in the assembly are assumed to behave according to Hooke's law. The parameters are summarised in Table 3.

Table 3: Material properties of the individual components used for the impact analyses.

Material	Young's modulus [GPa]	Poisson's ratio [-]	Density [kg/m <sup>3</sup> ]
Silicon	150.0	0.17	$2.3 \cdot 10^{-3}$
FR4	19.3	0.145	$2.6 \cdot 10^{-3}$
PA6	3.4	0.35	$1.1 \cdot 10^{-3}$
Solder	30.0	0.345	$8.4 \cdot 10^{-3}$

## Results

The analyses are carried out for three different configurations:

1. A PA6 housing on an FR4 carrier without chips.
2. A PA6 housing on an FR4 carrier with two chips attached to the housing as shown in Figure 11.
3. Two stacked PA6 housings on an FR4 carrier without any chips.

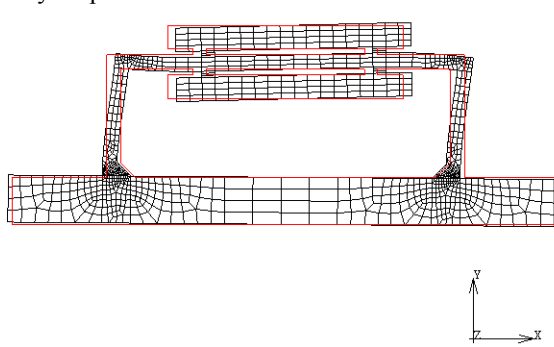


Figure 12: Deformed assembly of one housing and two chips (configuration 2) at  $4 \cdot 10^{-5}$  seconds after impact.

The maximal Von Mises strains during impact are comparable for the three investigated situations (a few MPa above the yield stress of the solder material). On the other hand, the total equivalent plastic strain is about a third lower for situation 3 than for situation 1 and 2.

The presented model gives a first impression of the impact behaviour of a stacked assembly. The impact simulations are ultimately aimed at determining the stresses in the solder joints during impact. For this, the current plane strain model needs further refinement.

## 5. Conclusions and future outlook

Finite element simulations were carried out to investigate the thermal and mechanical performance of the basic construction elements of the 3D MSP concept.

The relatively simple models gave a good initial insight in the thermal performance of some assemblies incorporating one or more chips. It is expected that the maximum dissipation power of chips must be well below 0.1W for the current package configurations in order to keep the maximum temperatures at an acceptable level. Even at 0.1W dissipation power, additional measures are possibly necessary to keep the maximum temperatures within limits.

Further investigations include the refinement of the impact model and an investigation of the thermo-mechanical reliability of the packages both by means of physical testing and numerical simulations.

## References

1. Bird, R.B., Stewart, W.E., Lightfoot, E.N., Transport Phenomena, Wiley (New York, 1960).
2. Hewitt, G.F., Shires, G.L., Bott, T.R., Process Heat Transfer, CRC Press (New York, 1994).
3. MSC.Marc, Manual, Vol. A–D (2001), MSC Software Corporation, <http://www.mssoftware.com>.
4. Wiese, S., Rzepka, S., Meusel, E., "Time-Independent Elastic-Plastic Behaviour of Solder Materials", *Proc. EuroSimE 2002*, Paris, France, April 2002, pp. 79–85.