



Point-One

Pole of innovative technology on nanoelectronics and embedded systems

MEMSLand

Cost Effective MEMS to Develop a Sustainable High Tech Business

Wafer-level Capping of MEMS Devices

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Motivation

Cost-effective, chip scale & generic

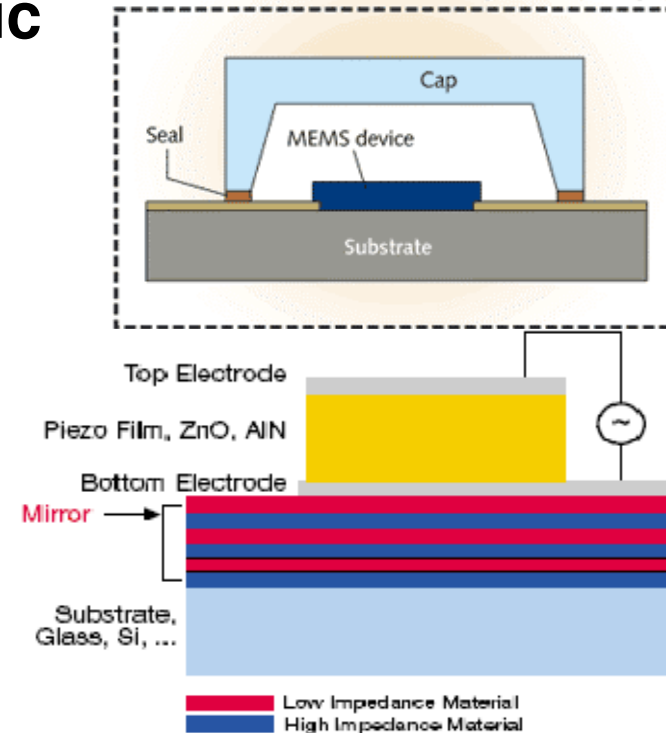
Standard processes, IC Fab

Comply with standard Packaging

BAW is taken as a vehicle

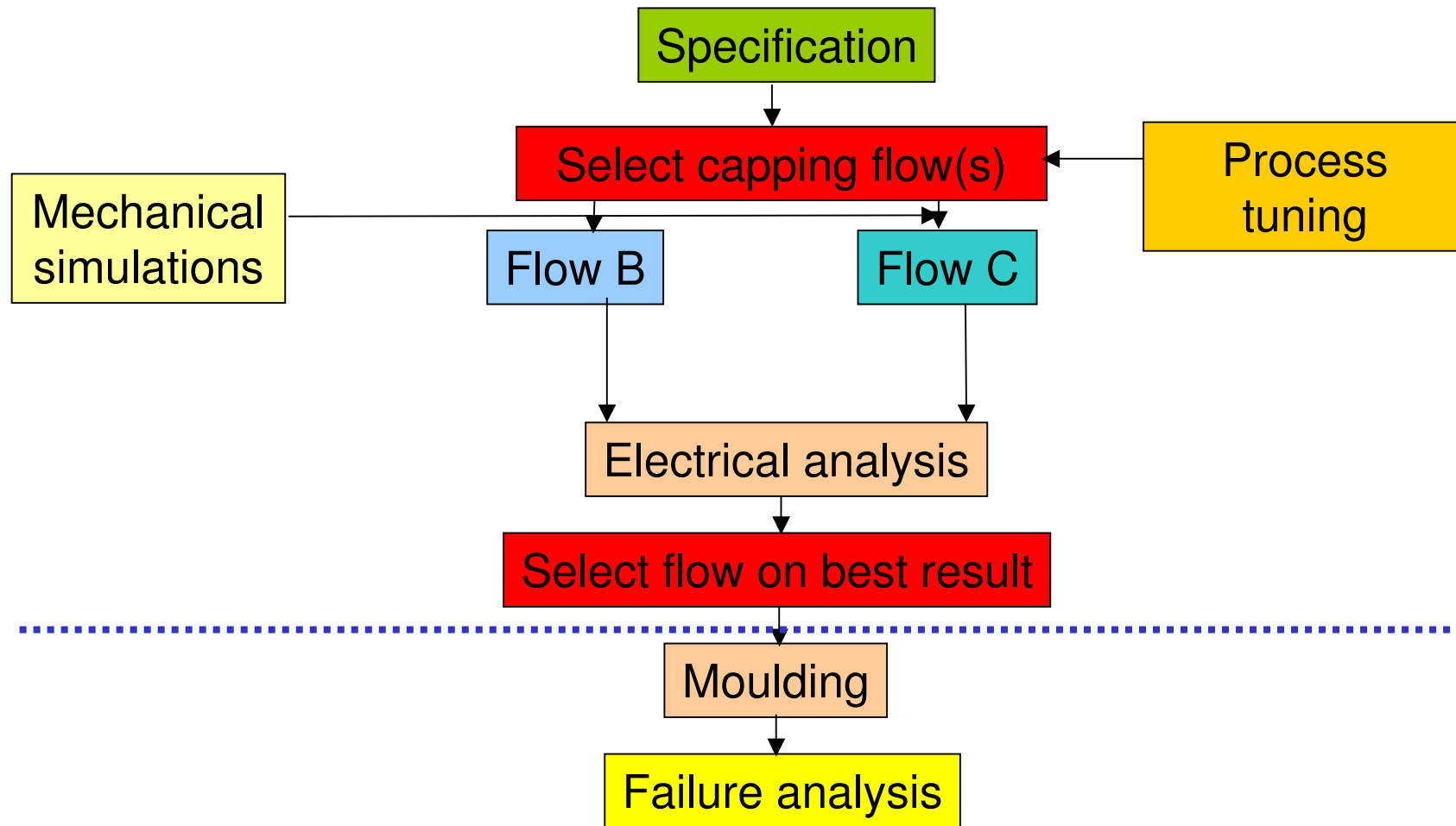
Wafer-level cap?

Higher-level packaging



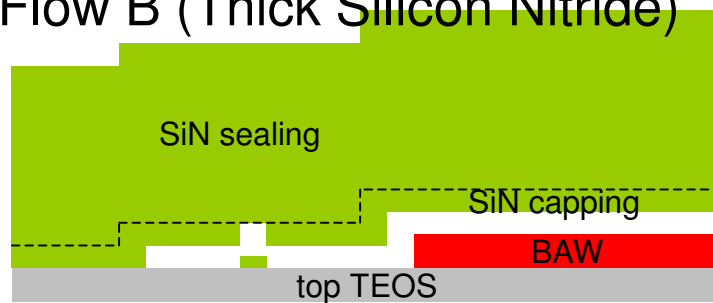
Feasibility, both at Wafer-level & Package-level

Project flow

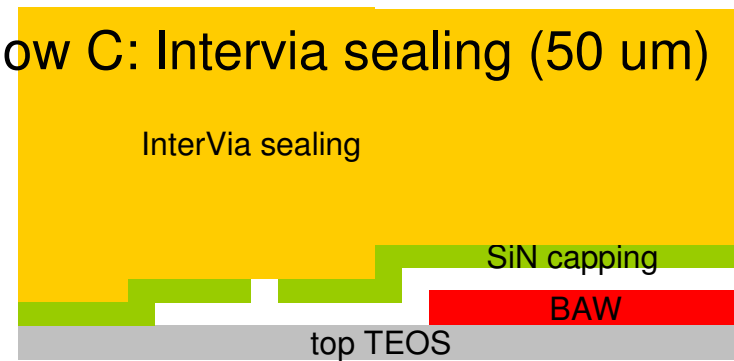


Capping routes

Flow B (Thick Silicon Nitride)

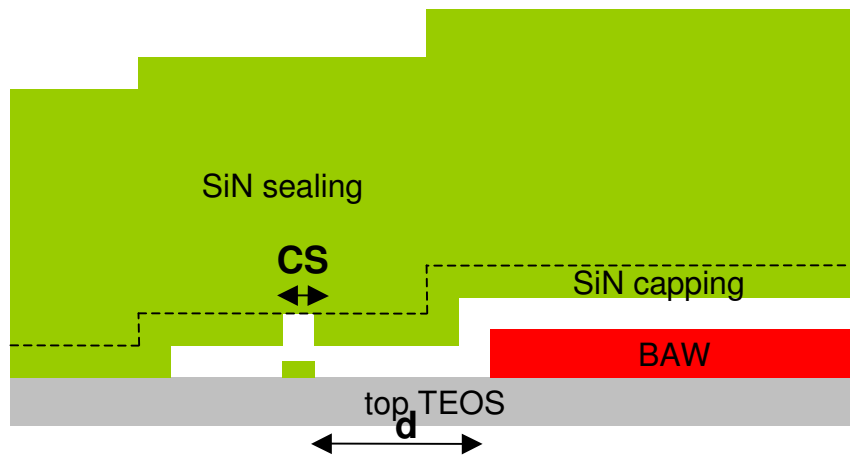


Flow C: Intervia sealing (50 um)

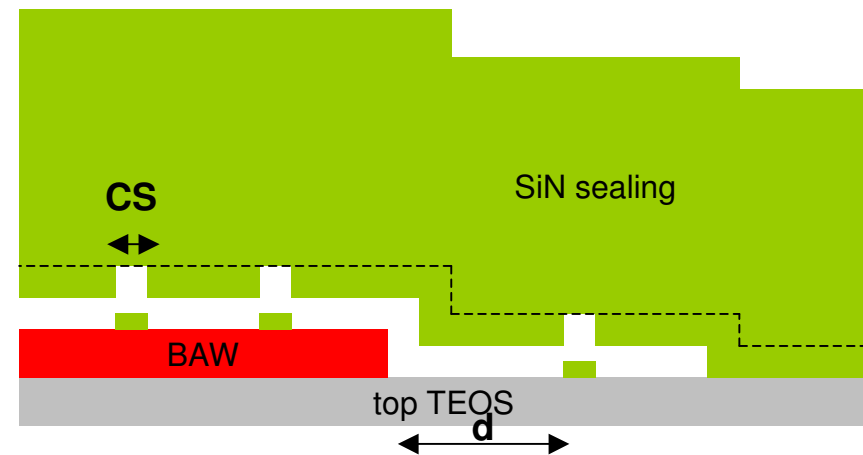


Design

Release holes outside active



Release holes above active

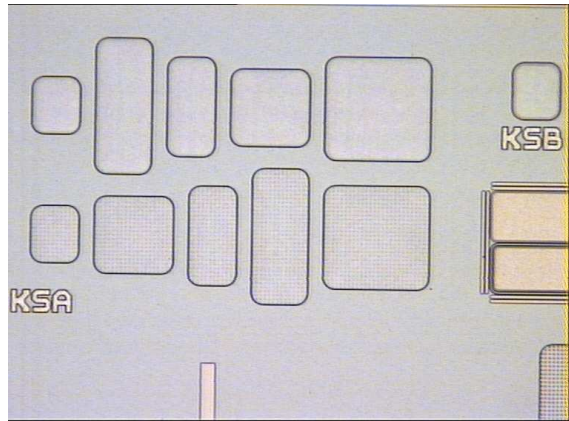


Design matrix $f(d, CS)$

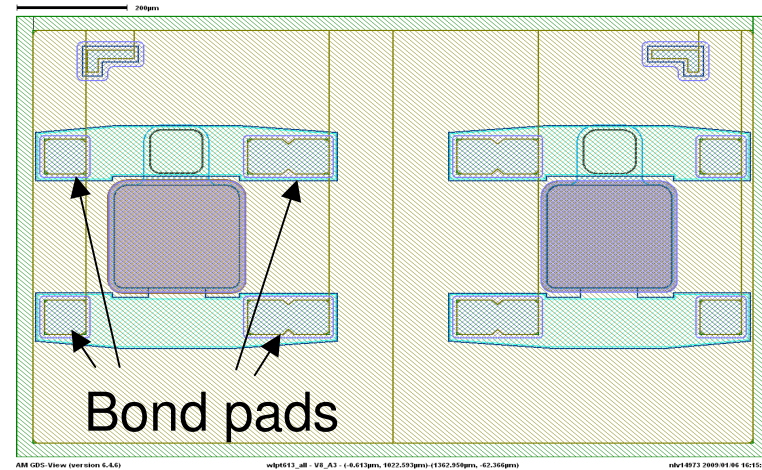
CS = release hole opening

d = distance release holes to active

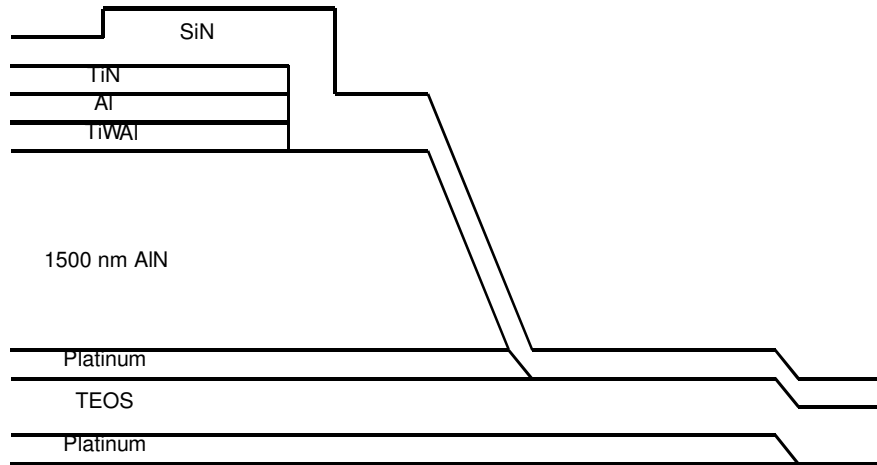
Modules



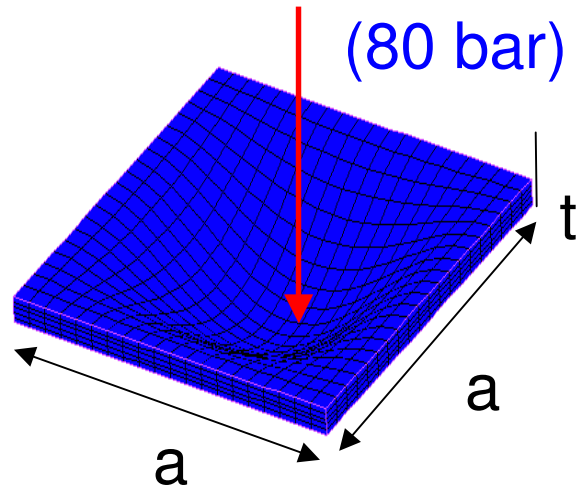
To study cavity *touch down*



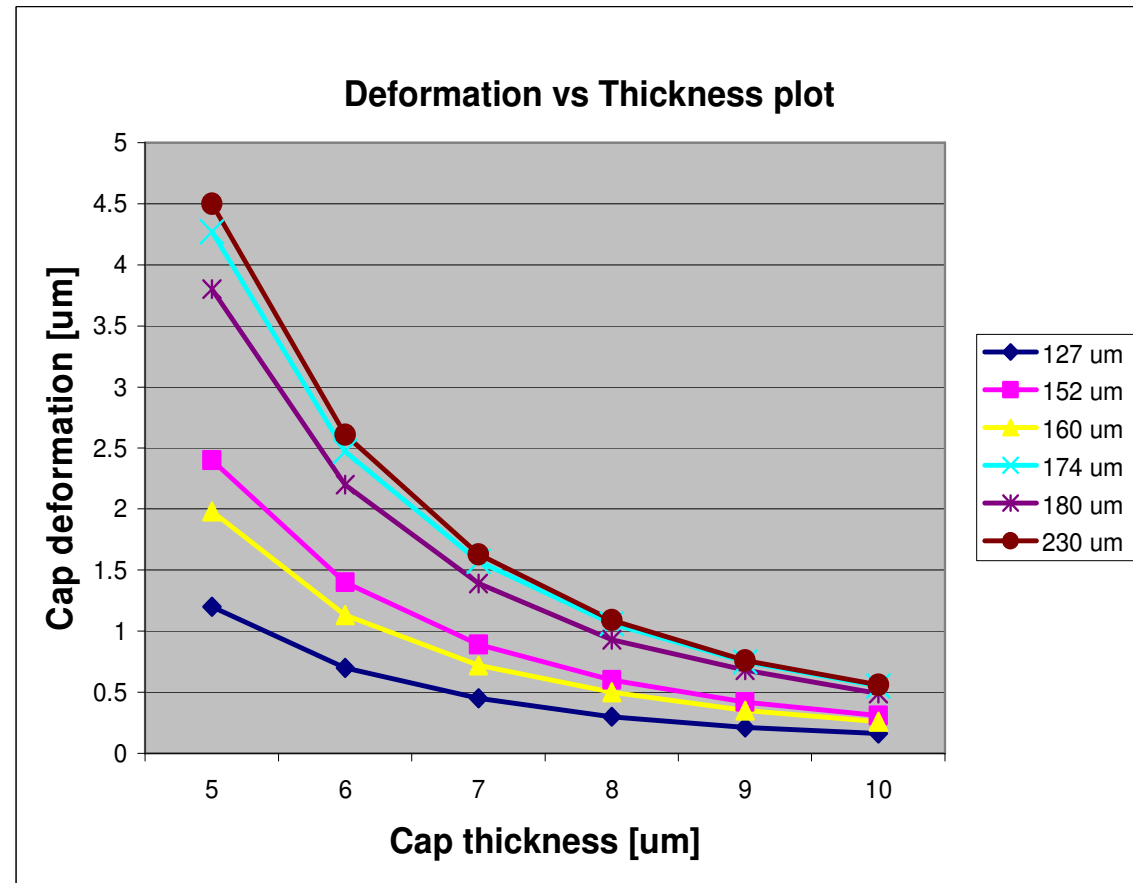
To demonstrate feasibility



Mechanical Simulations

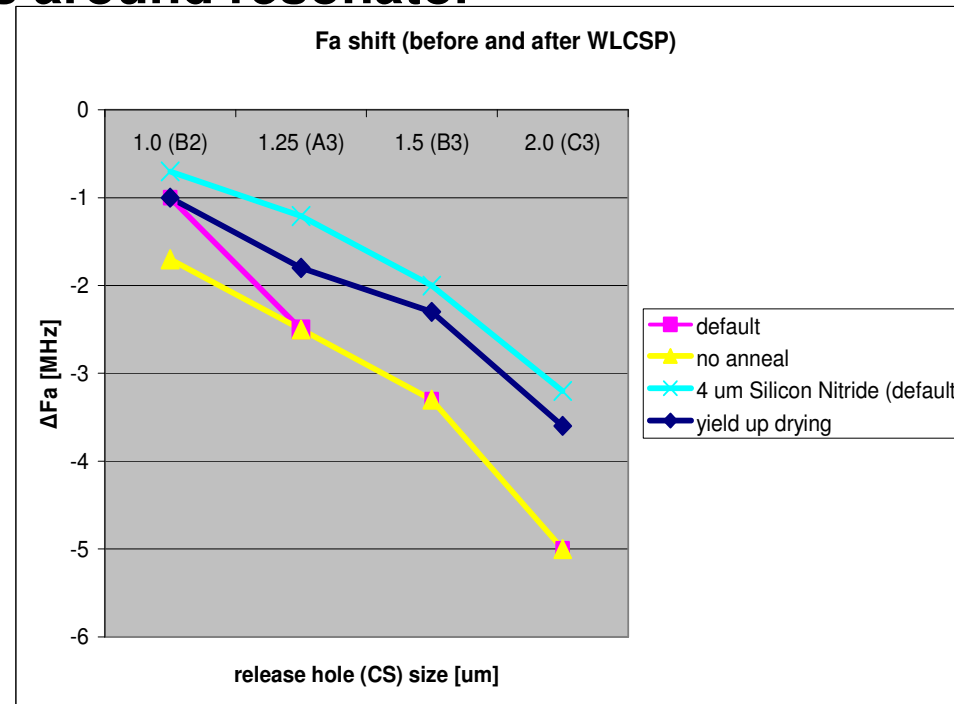
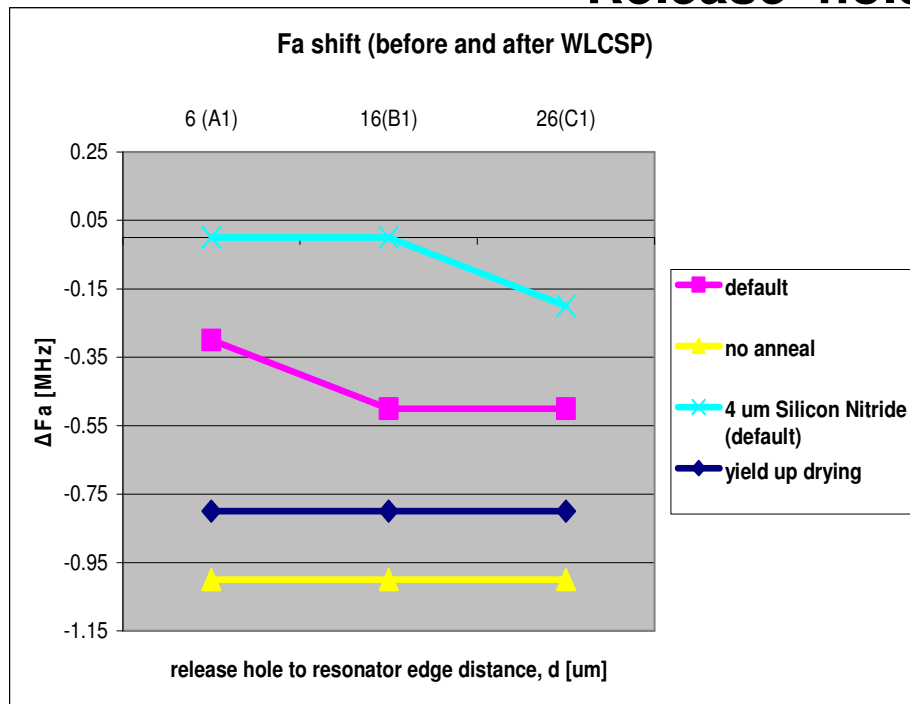


$$y = \frac{0.0138 \cdot q}{E} \times \left(\frac{l^4}{t^3} \right)$$



Results: Electrical Analysis

Release holes around resonator



Δ Fa shift is independent of the release hole distance

Larger the release hole size, larger becomes the Δ Fa shift

Packaging reliability Analysis

Why?

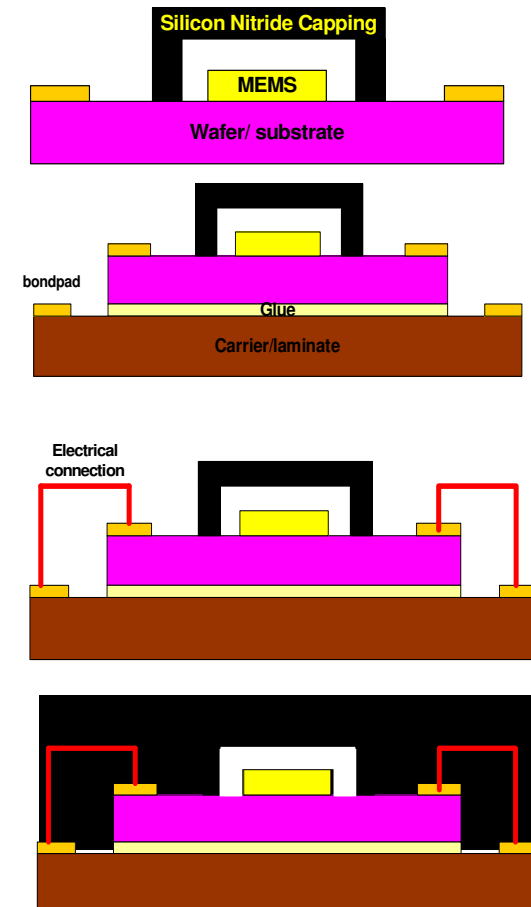
Package-level reliability testing

What?

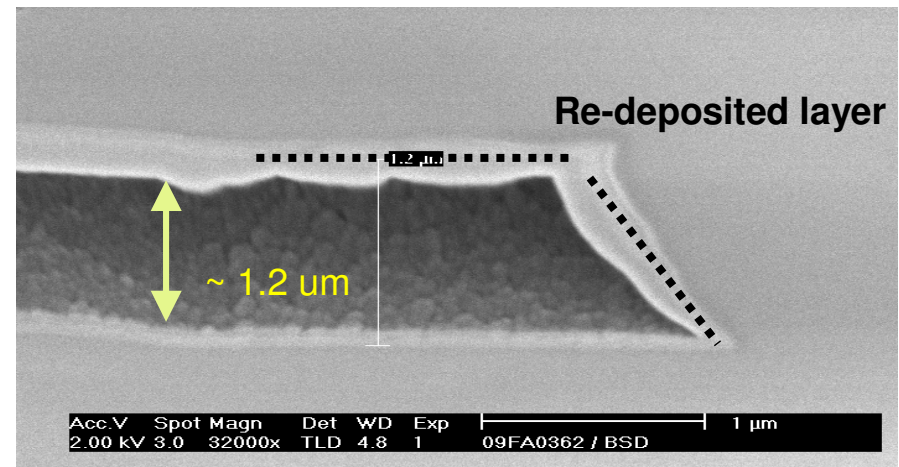
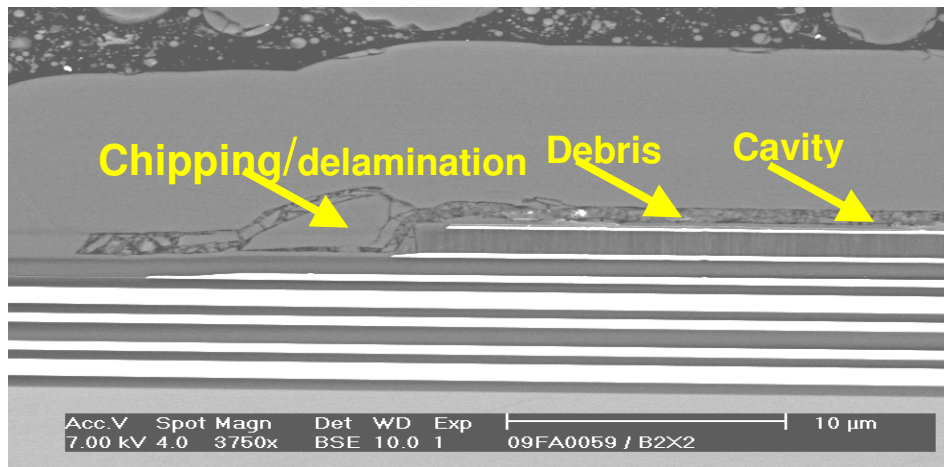
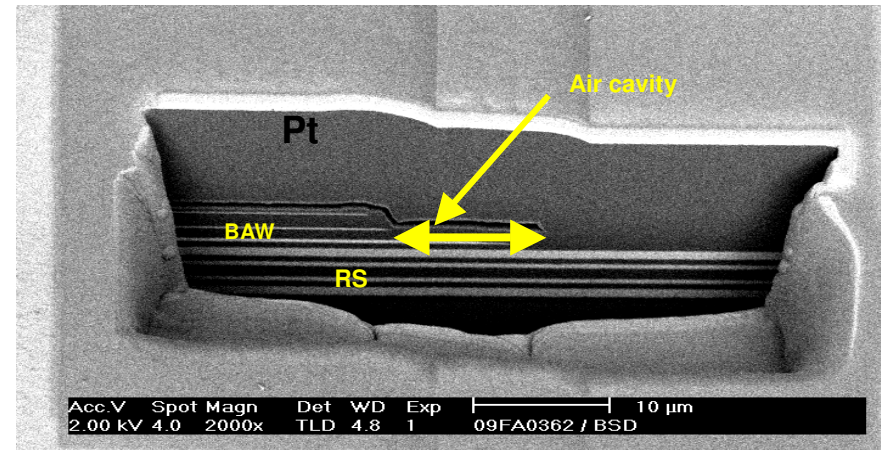
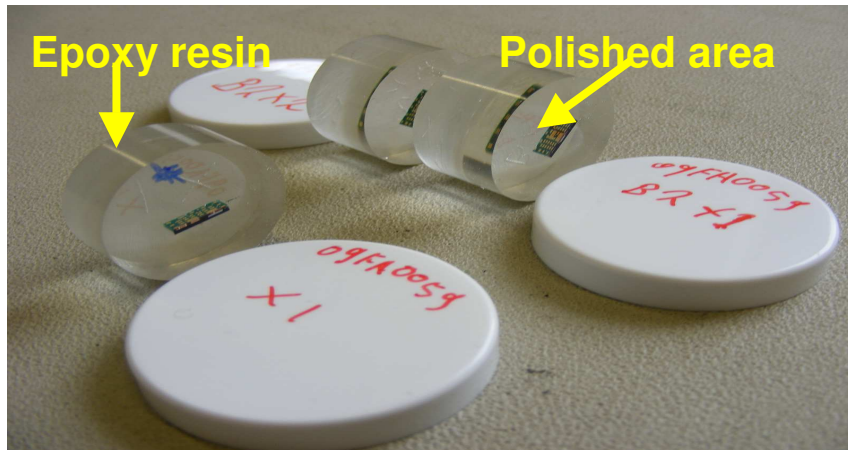
impact of moulding on the wafer-level cap
(Cracks, delamination and chipping)

How?

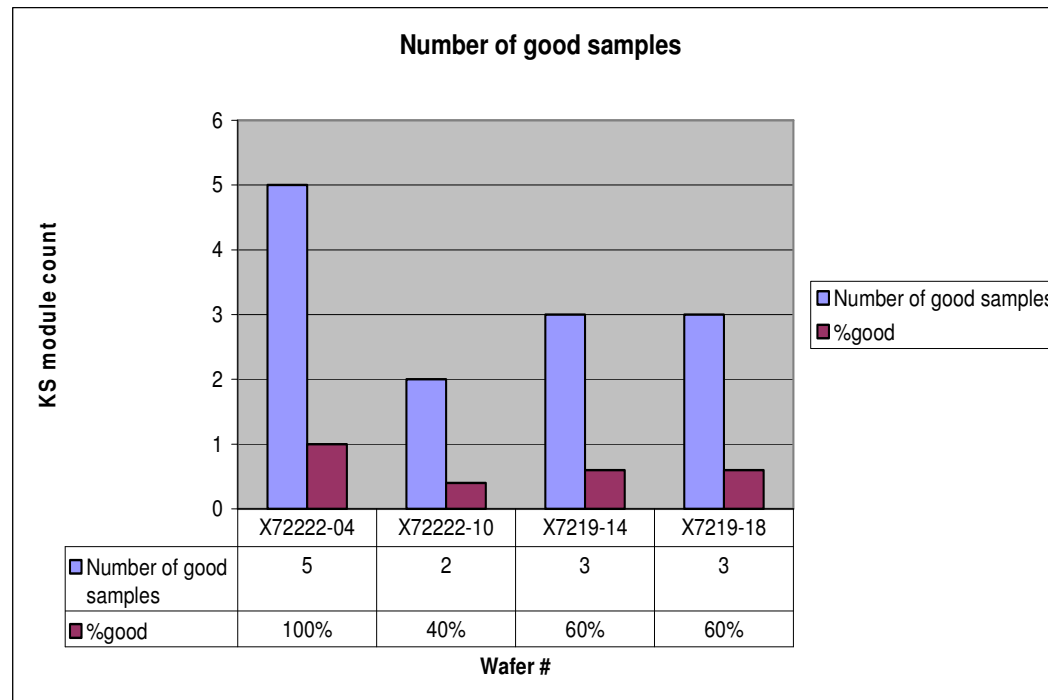
Cross section & decapsulation analysis



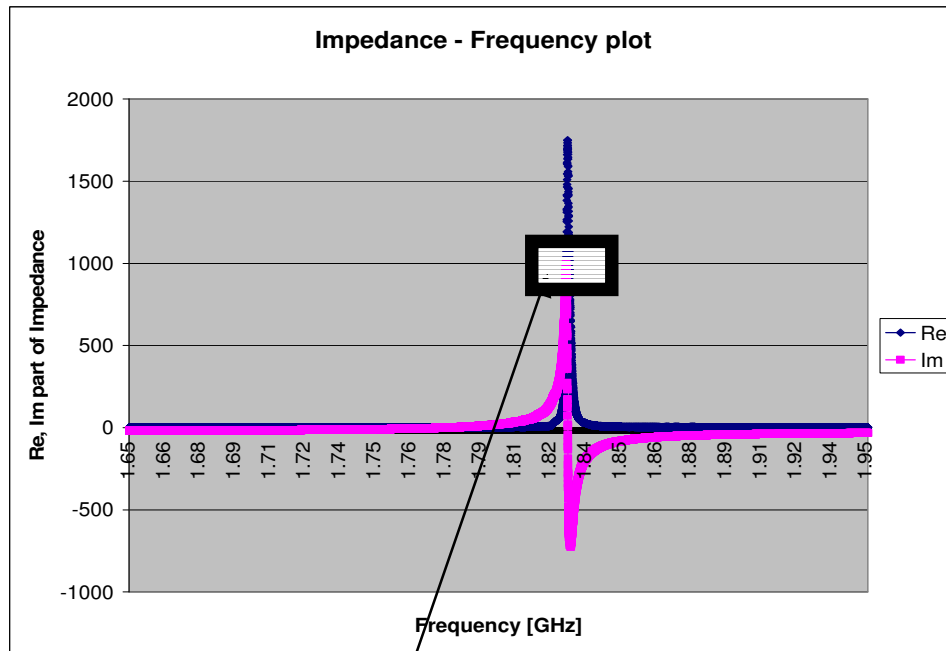
Structural Analysis



Risk: detaping



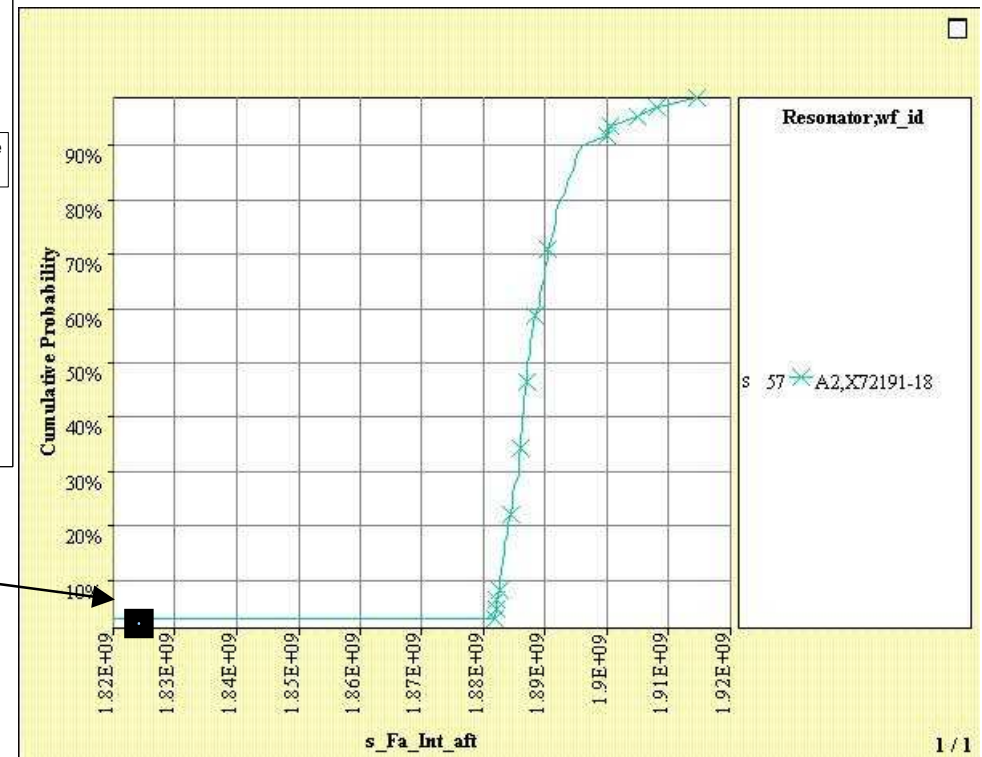
Electrical measurements: post-Moulding



Fa, Real : 1.828 GHz

~ 6 MHz deviation (large without tuning)

Fa shift after wafer-level processing



Conclusions: Mechanical

- Polishing results in debris and chipping off
- In FIB, re-deposition takes place in cavity
- **Capping survives moulding**

“BAW is electrically functional after moulding”

Summary

- **Two capping routes have been tried**
Thick Silicon Nitride,
Thin Silicon Nitride + Thick Intervia polymer
- **Capping route B -best option**
(Only release holes outside active, to avoid mass loading)
small release holes
- **Only standard wafer fab tools required**
- **Capping withstands moulding without collapsing**