56 MHZ PIEZORESISTIVE MICROMECHANICAL OSCILLATOR

J.J.M. Bontemps[*,1,2], *A. Murroni*[2], *J.T.M. van Beek*[2], *J.A.T.M. van den Homberg*[**,2], *J.J. Koning*[2], *G.E.J. Koops*[3], *G.J.A.M. Verheijden*[3], *J. van Wingerden*[2], *K.L. Phan*[2], *P. Vermeeren*[2], *C. van der Avoort*[2], *H.C.W. Beijerinck*[1], *P.G.M. Baltus*[1]
[1]Eindhoven University of Technology, The Netherlands
[2]NXP Semiconductors Netherlands
[3]NXP Semiconductors Belgium

ABSTRACT

A fully functional oscillator has been developed, based on a resonator with an electrostatic-to-piezoresistive transduction. Both resonator and amplifier IC have been processed on a SOI wafer with identical SOI layer thickness of 1.5 μm. The resonator is a bulk-acoustic 'dogbone' design, for which an extended electrical model is presented. At an oscillation frequency of 56.1 MHz the oscillator consumes 6.1 mW and reaches a phase noise of -102 dBc/Hz at 1 kHz offset from carrier.

KEYWORDS

Reference oscillator, piezoresistive, MEMS resonator, silicon-on-insulator technology (SOI), phase noise.

INTRODUCTION

Mechanical resonators are widely applied in time-keeping and frequency reference applications. Mechanical resonators are preferred over electrical resonators because of their high Q. Quartz crystals are still ubiquitous in electronic equipment, showing excellent performance in terms of stability (short-term and long-term), power handling and temperature drift.

Micromechanical resonators have been researched as a potential alternative to the bulky quartz crystals, which cannot be integrated with IC technology. Efforts over recent years have shown that micromechanical resonators are capable of high Q [1], low temperature drift [2], excellent phase noise performance with low power consumption [3], and show almost no long term drift when packaged [4].

Most resonators use capacitive transduction to excite and detect the mechanical resonance, because it is easily implemented on-chip. These resonators typically suffer from high impedance at resonance. Several approaches have been explored to lower the impedance by decreasing the gap width, increasing the aspect ratio of the gap, or using piezoelectric actuation. A disadvantage of all these methods is that they increase manufacturing complexity.

A new approach presented by van Beek et al. [5] combines electrostatic actuation with piezoresistive readout. This approach allows for low effective impedance and is insensitive to geometric scaling or layer thickness [5,6]. The resonators can thus be made in a thin layer that allows for surface micro machining. This paper presents a MEMS oscillator at 56.1 MHz, based on a resonator with an electrostatic-to-piezoresistive transduction.

RESONATOR

Process & Design

The resonator is processed on a silicon-on-insulator (SOI) wafer. The resonator is reactive ion etched into a 1.5 μm thick, n-type, SOI layer down to the buried oxide layer. Next, the resonator is released by isotropic etching of the buried oxide layer with HF vapor.

For the 'dogbone' design [7], the dimensions and selected eigenmode are depicted in figure 1. The resonant system comprises two identical resonators that are connected back-to-back for a balanced operation mode and high Q [8]. The dogbone can be idealized as a mass-spring system. Two springs of length L and width w are separated by a slit to redirect the current along the springs. The lumped mass head of length a and width b increases the electrode area of the resonator. Moreover, the strain of the resonator is concentrated in the springs. The dimensions of the resonator are depicted in figure 1 and table 1.

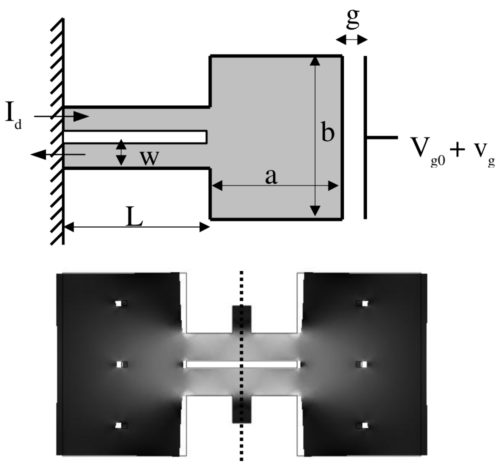

Figure 1: Top view of the dogbone resonator showing the dimensions of the design (top, half device) and the selected eigenmode simulated in Comsol (bottom, full device). The lateral strain is simulated where light areas correspond to regions of high strain.

[**] Now at ASML Netherlands

Model

The electrical behavior of the resonator is identical to a field-effect transistor in the linear region with frequency selectivity. The model therefore incorporates a transconductive element that is frequency dependent:

$$g_m = \frac{g_{m0}}{\left(1 - \frac{f^2}{f_0^2} + j\frac{f}{Qf_0}\right)} \qquad (1)$$

$$g_{m0} = -V_{dc} I_d \frac{4\varepsilon_0}{\pi^2}\frac{K}{E}\frac{1}{g^2}\frac{b}{w}\alpha$$

where ε_0 is the dielectric constant, f_0 the resonance frequency, K the piezoresistive gauge factor, E the Young's modulus, g the actuation gap width, and α a factor that accounts for the amount of strain concentration in the springs. The electrical equivalent model of the resonator is depicted in figure 2.

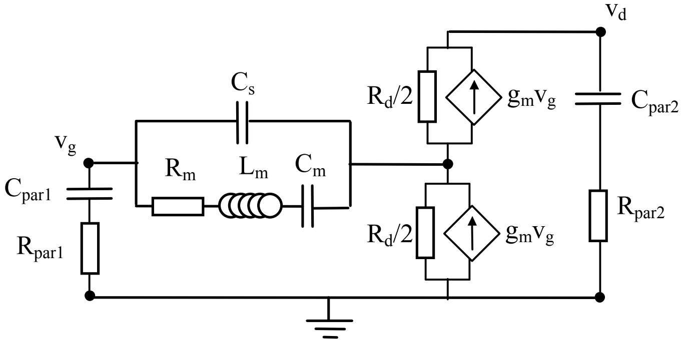

Figure 2: The MEMS resonator small signal model with the piezoresistive behavior modeled as a resonant transconductive element g_m. This signal is superimposed on the capacitive signal modeled with the R_m-L_m-C_m branch (see table 1 for symbols).

Measurements

The resonator response has been measured on an Agilent E5062A ENA-L network analyzer. The measured data has been fitted with the electrical small signal model in figure 2 to extract the model parameters. In figures 3 and 4 it can be seen that the model generates an excellent fit to the measured data.

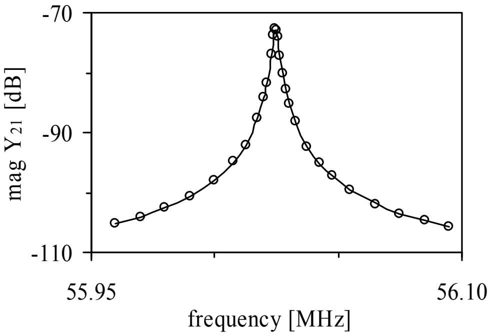

Figure 3: Magnitude of the measured Y21 parameter of the piezoresistive resonator, V_g=20V and I_d=1mA.

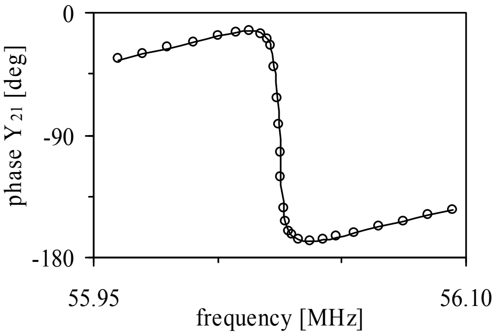

Figure 4: Phase of the measured Y21 parameter for the piezoresistive resonator, V_g=20V and I_d=1mA.

With a b/w ratio of 6.7 and a α of 2 the resonator shows a transconductance of 0.19 mS at resonance. The parallel combination of the resonator resistance R_d and the bondpad capacitance C_{par2} load the g_m. Care in the design is taken to keep the value of C_{par2} as low as possible to reduce phase shift and drop in gain, resulting in a measured value for C_{par2} of 200 fF.

The gain of the resonator is linearly proportional to the product of the gap voltage V_{dc} and the bias current through the resonator I_d. Note that the bias voltage applied on the electrodes V_g is higher then the gap voltage V_{dc}. This is due to the current I_d that lifts the potential of the resonator. For V_g=20V and I_d=1mA the measured gain of the resonator is –10 dB with a phase shift of 68°. Table 1 summarizes the extracted electrical parameters from the measurements.

Table 1: Dimensions of the dogbone resonator and characteristic parameters extracted from measurements. The electrical model of the resonator can be found in fig 2.

Parameter	***Symbol***	***Value***	***Units***
Spring length	L	6.0	[μm]
Spring width	w	3.0	[μm]
Mass head length	a	13.4	[μm]
Mass head width	b	20.0	[μm]
Transducer gap	g	0.27	[μm]
Effective mass	m_{eff}	1.66	[ng]
Effective spring constant	k_{eff}	207	[kNm]
Resonance frequency	f_{res}	56.1	[MHz]
Quality factor	Q	30k	
Electrode bias voltage	V_g	20	[V]
Bias current	I_d	1	[mA]
Motional resistance	R_m	516	[kΩ]
Motional inductance	L_m	32.2	[H]
Motional capacitance	C_m	0.25	[aF]
Shunt capacitance	C_s	16.5	[fF]
Piezo resistance	R_d	1.98	[kΩ]
Parasitice capacitance	C_{par2}	192	[fF]
Transconductance	g_{m0}	6.20	[nS]
Transconductance at resonance	$g_{m,max}$	0.19	[mS]
Gain	A_v	-10.0	[dB]
Phase	φ	68	[deg]

OSCILLATOR CIRCUIT DESIGN

The amplifier chip has been designed in the ABCD2 process [9] on a SOI wafer with identical SOI layer thickness of 1.5 µm. The ABCD2 process has been chosen, because of the process high voltage capability. High voltage is needed for the electrode bias voltage of the resonator.

The amplifier design consists of an output buffered, two-stage amplifier that operates at 3V. The two identical gain stages and the output buffer have been entirely designed with lateral npn bipolar transistors. Bipolar transistors have a superior noise performance over MOS devices. A disadvantage is that the bipolar transistors in the ABCD2 process have low speed (f_T=200 MHz). The core of the gain stage (figure 5) is a cascaded common-collector common-emitter configuration, also known as a CC-CE cascade

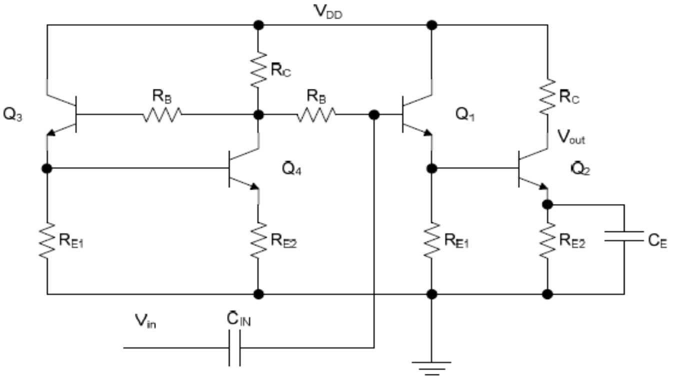

Figure 5: The gain stage of the ABCD2 amplifier. The input signal V_{in} is decoupled via the input capacitance C_{in}, which also provides the stage with a high pass response. Left from the point where V_{in} connects to the circuit is the replica bias circuit. Right from this point is the CC-CE cascade.

Two stages are needed, since with a single stage the required gain and phase could not be achieved. The gain of the single stages has been improved by replacing all MOS biasing current mirrors by resistors. This decreases the total capacitance to ground, which improves the limited gain-phase performance of the amplifier.

The amplifier circuit is biased with a replica bias technique. The bias is determined by a replica of the amplifier circuit, which is self-biased through a negative feedback loop. The negative feedback guarantees stability of the bias against temperature and process variations.

An on-chip current mirror is designed to supply the bias current to the resonator. If the current would be supplied externally, the drain of the resonator needs to be connected to an external pin. This would load the resonator and cause a significant drop in resonator gain.

Measurements on the amplifier IC show that the amplifier is able to deliver 20 dB gain at a phase shift of -70°. The layout of the amplifier design, which is about 1 mm^2 in size, is depicted in figure 6.

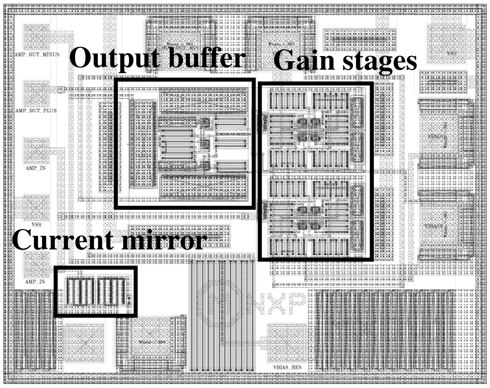

Figure 6: The mask layout of the ABCD2 amplifier chip. Size of the chip is 0.97 x 1.22 mm^2.

OSCILLATOR MEASUREMENTS

For the piezoresistive oscillator, the amplifier die and the resonator die are wire bonded together in a ceramic DIL-24 package. A small PCB enables the power supply to the circuit and the electrode bias voltage for the resonator, which are applied externally.

From the fifteen bonded oscillator samples, all are functional. For the resonators the yield on wafer is close to 100% for this design.

As has been explained, the gain of the resonator is proportional to the product of gap voltage and bias current. Therefore, the two are interchangeable, where an increase in bias current leads to a higher power consumption of the resonator.

For the oscillator measurements in vacuum, oscillation is sustained for an electrode bias voltage as low as 7.2V with a bias current of 2 mA. Conversely, the bias current can be reduced to 0.5 mA with an electrode bias voltage of 20V. Oscillation can be sustained to a pressure of 440 mbar, with V_g=30V and I_d=2 mA.

Typical bias conditions are 15V electrode bias voltage and 0.74 mA bias current, which result in a total power consumption for the oscillator of 6.1 mW.

Table 2: Specifications of the 56 MHz piezoresistive *oscillator.*

Parameter	*Symbol*	*Value*	*Units*
Oscillation frequency	f_{osc}	56.1	[MHz]
Power consumption	P_{tot}	6.2	[mW]
Amplifier	P_{amp}	5.1	
Resonator	P_{res}	1.1	
Operation voltage	V_{DD}	3.0	[V]
Gate voltage	V_g	15	[V]
Startup time	t	1.0	[mS]
Phase noise performance			
10 Hz	L_f	-48	[dBc/Hz]
1 kHz		-102	[dBc/Hz]
Floor		-113	[dBc/Hz]

The phase noise performance of the oscillator is measured with an Agilent E5052B Signal Source Analyzer. We measure a phase noise of –102 dBc/Hz at 1 kHz offset from carrier and –113 dBc/Hz floor at far from carrier offsets (figure 7). In order to compare with state-of-the-art performance [3], the measured 1 kHz point needs to be translated from 56 MHz to 13 MHz. If the frequency is divided down, this translates into –115 dBc/Hz at 1 kHz from a 13 MHz carrier. This is higher than best-in-class capacitive MEMS oscillators that achieve –130 dBc/Hz at 1 kHz from carrier.

The near-carrier spectrum shows a drop of 30 dB/decade. This is a clear indication of 1/f noise intermodulation around the carrier. This degrades the near-carrier noise performance. Furthermore, the phase noise performance suffers from a low signal level in the oscillator core. By increasing the signal level inside the oscillator core and decreasing the 1/f noise added by the circuit components, phase noise performance of the piezoresistive oscillator can still be improved.

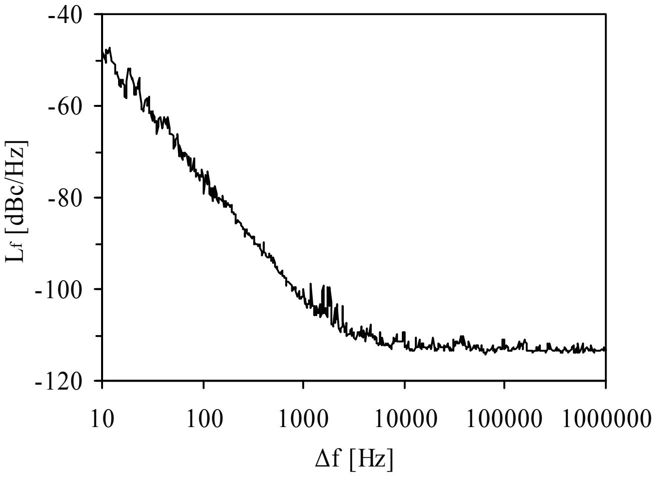

Figure 7: The phase noise spectrum of the oscillator measured at bias settings V_g*=12.6V &* I_d*=0.7mA.*

CONCLUSION

Piezoresistive resonators are insensitive to geometric scaling and layer thickness. The piezoresistive resonators can therefore be surface micro-machined in thin silicon layers, which is compatible with standard IC processing. Moreover, they are very attractive for high-frequency oscillators. In this paper we have demonstrated a fully functional MEMS oscillator at 56.1 MHz, based on a resonator with an electrostatic-to-piezoresistive transduction.

The oscillator consumes 6.1 mW and exhibits a phase noise of –102 dBc/Hz at 1 kHz offset from carrier and –113 dBc/Hz at far from carrier offsets. This demonstrates feasibility of the piezoresistive MEMS oscillator for low-power, low-noise applications.

ACKNOWLEDGEMENTS

The authors would like to thank MEMSland for the financial contribution to the project. MEMSland is an initiative of the Dutch Department of Economic Affairs on MEMS innovation. Gerrit den Besten is acknowledged for his support on the phase noise measurements.

REFERENCES

[1] L. Khine, M. Palaniapan, W.-K. Wong, "6 MHz bulk-mode resonator with Q values exceeding one million", in *Digest Tech. Papers Transducers 2007*, Lyon, 10-14 June, 2007, pp. 2445-2448.

[2] G.K. Ho, K. Sundaresan, S. Pourkamali, F. Ayazi, "Temperature compensated IBAR reference oscillator", in *Digest Tech. Papers MEMS 2006*, Istanbul, 22-26 January, 2006, pp. 910-913.

[3] V. Kaajakari et al., "Low noise silicon micromechanical bulk acoustic wave oscillator", in *Digest Tech. Papers IEEE Ultrasonics Symposium*, 18-21 September, 2005, pp. 1299-1302.

[4] M.A. Hopcroft et al., "A high-stability MEMS frequency reference", ", in *Digest Tech. Papers Transducers 2007*, Lyon, 10-14 June, 2007, pp. 1307-1310.

[5] J.T.M. van Beek, P.G. Steeneken, B. Giesbers, "A 10 MHz piezoresistive MEMS resonator with high Q", in *Digest Tech. Papers International Frequency and Control Symposium and Exposition*, Miami, June 4-7, 2006, pp. 475-480.

[6] J.T.M. van Beek et. al., "Scalable 1.1 GHz fundamental mode piezo-resistive silicon MEMS resonators", in *Digest Tech. Papers IEDM 2007*, Washington DC, December 10-12, 2007, pp. 411-414.

[7] J.T.M. van Beek et. al., "A piezo-resistive resonant MEMS amplifier", in *Digest Tech. Papers IEDM 2008*, San Francisco, December 15-17, 2008, pp. 667-670.

[8] T. Matilla et. al., "A 12 MHz micromechanical bulk acoustic mode oscillator", *Sensor and Actuators A*, vol. 101, pp. 1-9, 2002.

[9] J.A. van der Pol et. al., "A-BCD: An economic 100 V RESURF Silicon-On-Insulator BCD Technology for Consumer and Automotive Applications", in *Proc. ISPSD 2000*, Toulouse, May 22-25, 2000, pp. 327-330.

CONTACT

* J.J.M. Bontemps, tel: +31-24-3534019;
joep.bontemps@nxp.com